**Amendments to the Claims**

This listing of claims will replace all prior versions and listing of claims in the application:

1. (Original): A digital pulse-width-modulation (PWM) generator comprising:

an n bit digital magnitude comparator having first and second n bit inputs and an output indicative of the relative values of the signals applied at the first and second inputs;

a first n bit digital up/down counter having a count direction input coupled to receive a sign bit of a digital unary input signal, an n bit parallel binary count output connected to the first n bit input of the magnitude comparator, and a clock input;

a second n bit counter having a clock input coupled to receive a constant rate clock signal and an n bit parallel binary count output connected to the second n bit input of the magnitude comparator;

an AND gate having a first input coupled to receive the constant rate clock signal in frequency divided form and a second input coupled to receive a magnitude portion of the digital unary input signal, and further having an output connected to the clock input of the first counter; and

wherein the comparator continually generates an output signal indicative of the relative magnitudes of the counts of the first and second counters, whereby said output signal is PWM output signal with an average value representing a ramp voltage having a slope determined by magnitude portion of the digital unary input signal with a direction of a slope of the output signal being determined by the polarity of the sign bit.

2. (Original): A digital pulse-width-modulation (PWM) generator as claimed in claim 1, wherein the n bit parallel binary count output of the first n bit digital up/down counter is connected to the first n bit of the magnitude comparator with a least significant bit (LSB) of the output connected to a LSB of the first input of the comparator and thereafter in bit significance sequence, and the n bit parallel binary count output of the second n bit counter is connected to the second n bit input of the magnitude comparator with a LSB of the output connected to a LSB of the second input of the comparator and thereafter in bit significance sequence.

3. (Original): A digital pulse-width-modulation (PWM) generator as claimed in claim 1 wherein the n bit parallel binary count output of the second n bit digital up/down counter is connected to the second n bit input of the magnitude comparator with a most significant bit (MSB) of the output connected to a LSB of the second input of the comparator and thereafter in reverse bit significance sequence, and the n bit parallel binary count output of the first n bit counter is connected to the first n bit input of the magnitude comparator with a LSB of the output connected to a LSB of the first input of the comparator and thereafter in bit significance sequence.

4. (Original): A digital pulse width modulation generator comprising an up/down digital counter, a digital magnitude comparator, and a second digital counter, wherein the magnitude comparator compares the relative sizes of the counts in the two counters connected to the magnitude comparator in the conventional sense with least significant bit outputs connected to least significant bit inputs of the comparator and thereafter in bit significance sequence, and whose greater-than or less-than outputs provide pulse width modulation signals, when the second counter is clocked continuously by a constant rate

clock signal and when the up/down input of the up/down counter is controlled by the sign bit of the digital input signal and the clock input of the up/down counter is gated on and off by the presence or absence of the unary input signal wherein the pulse width modulated output signal or signals convert a steady pulse on the unary input into a pulse width modulated ramp at the output, the slope of the ramp being determined by the polarity of the sign bit input.

5. (Original): A digital pulse width modulator as claimed in claim 4 except that the outputs of the second counter are connected to one of the input ports of the magnitude comparator in bit-reversed order that is in the reverse of the conventional ordering of bits and in particular with the least significant bit output of the counter connected to the most significant bit input of the comparator and vice versa, such that the pulse width modulated output from the comparator now makes many more transitions per total count cycle of the second counter whilst still maintaining the required average mark:space ratio, thus easing the usually required low pass filtering of the pulse width modulated output.

6. (New): A digital pulse width modulation generator for pulse width modulating a digital input signal comprising a single data bit and a sign bit, comprising:

an up/down digital counter (46), the up/down input of the up/down counter (46) being controlled by the sign bit of the digital input signal;

an AND gate (45) having a first input which is clocked continuously by a first clock signal, a second input which receives the data bit of the digital input signal, and an output connected to the clock input of the up/down counter (46);

a second digital counter (42) clocked continuously by a constant rate,

second clock signal;

a digital magnitude comparator (43) which compares the outputs of the two counters (42, 46) so that the greater-than or less-than output of the magnitude comparator (43) provides a pulse width modulation output signal, whereby the value represented by the pulse width modulation output signal is a ramp when the data bit of the digital input signal is at logic one and is a static value when the data bit of the digital input signal is at logic zero, the slope of the ramp being determined by the polarity of the sign bit of the digital input signal.

7. (New): A digital pulse width modulation generator according to claim 6, wherein the outputs of the two counters (42, 46) are connected to the inputs of the magnitude comparator (43) with the bits of the outputs of the two counters (42, 46) connected to the bits of the inputs of the magnitude comparator (43) in bit significance sequence.

8. (New): A digital pulse width modulation generator according to claim 6, wherein:

the output of the up/down counter (46) is connected to an input of the magnitude comparator (43) with the bits of the output of the up/down digital counter (46) connected to the bits of the input of the magnitude comparator (43) with the bits in an order other than in bit significance sequence; and

the output of the second counter (42) is connected to an input of the magnitude comparator (43) with the bits in an order other than in bit significance sequence.

9. (New): A digital pulse width modulation generator according to claim 1, wherein:

the output of the up/down counter (46) is connected to an input of the magnitude comparator (43) with the bits of the output of the up/down digital counter (46) connected to the bits of the input of the magnitude comparator (43) in bit significance sequence, and

the output of the second counter (42) is connected to an input of the magnitude comparator (43) with the bits of the output of the second counter (42) connected to the bits of the input of the magnitude comparator (43) in reverse bit significance.

10. (New): A digital pulse width modulation generator according to claim 6, wherein the up/down counter (46) is a dead-end counter.

11. (New): A digital pulse width modulation generator according to claim 6, wherein the digital input signal is synchronized with said constant rate clock signal.

12. (New): A digital pulse width modulation generator according to claim 6, wherein the first clock signal is the second clock signal in frequency-divided form.

13. (New): A digital pulse width modulation generator according to claim 6, wherein the first and second clock signals are derived from different clocks.

14. (New): A digital pulse width modulation generator according to claim 6, wherein the up/down digital counter (46) has a reset input arranged to set the up/down digital counter (46) to half of the full count.